WHAT IS CLAIMED IS:

1. A buffer circuit mounted in a memory circuit and comprising:

a signal terminal;

a synchronous input buffer having an input coupled to said signal terminal;

an asynchronous input buffer having an input coupled to said input terminal; and

a switching circuit which selectively outputs an output of said synchronous input buffer or an output of said asynchronous input buffer according to an operational mode of the memory circuit.

2. The circuit of claim 1, wherein an output of the switching circuit enables and disables a termination resistance of the memory circuit.

3. The circuit of claim 2, wherein the switching circuit is responsive to an operational mode signal which is supplied externally of the memory circuit to selectively output the output of said synchronous input buffer or the output of said

asynchronous input buffer.

4. The circuit of claim 1, further comprising an operational mode detection circuit, wherein the switching circuit is responsive to an output of the operational mode detection circuit to selectively output the output of said synchronous input buffer or the output of said asynchronous input buffer.

5. The circuit of claim 3, wherein the operational mode signal is indicative of an active mode, a stand-by mode and a power-down mode of the memory circuit, and wherein a delay locked loop (DLL) circuit or a phase locked loop (PLL) circuit of the memory circuit is active when the memory circuit is in the active mode, and wherein the DLL circuit or the PLL circuit is inactive during the stand-by mode and the power-down mode.

6. The circuit of claim 4, wherein the switching circuit is responsive to an operational mode signal which is supplied externally of the memory circuit to

selectively output the output of said synchronous input buffer or the output of said asynchronous input buffer, wherein the operational mode signal is indicative of an active mode, a stand-by mode and a power-down mode of the memory circuit, and wherein a delay locked loop (DLL) circuit or a phase locked loop (PLL) circuit of the memory circuit is active when the memory circuit is in the active mode, and wherein the DLL circuit or the PLL circuit is inactive during the stand-by mode and the power-down mode.

7. The circuit of claim 2, wherein the switching circuit is responsive to a value stored in a mode register of the memory circuit to selectively output the output of said synchronous input buffer or the output of said asynchronous input buffer.

8. An active termination circuit mounted in a memory circuit and comprising:

a termination resistor which provides a termination resistance for the

memory circuit; and

a control circuit which receives an externally supplied active termination control signal, and which selectively switches on and off the termination resistor in response to the active termination control signal;

wherein said control circuit includes a synchronous input buffer and an asynchronous input buffer which each receive the active termination control signal, and a switching circuit which selectively outputs an output of said synchronous input buffer or an output of said asynchronous input buffer according to an operational mode of the memory circuit, and wherein an output of said switching circuit controls an on/off state of said termination resistor.

9. The circuit of claim 8, wherein the switching circuit selects the output of the synchronous input buffer when the memory circuit is in an active operational mode, and selects the output of the asynchronous input buffer when the memory circuit is in a standby or power-down operational mode.

10. The circuit of claim 8, further comprising a mode register which stores a value indicative of an operational mode of the control circuit, wherein the control circuit is deactivated when the operational mode of the control circuit is off, and wherein the control circuit is activated to output the output of said synchronous input buffer or the output of said asynchronous input buffer when the operational mode of the control circuit is on.

11. A memory system comprising:

a bus line;

a plurality of memory circuits coupled to said bus line;

a chip set, coupled to said bus line, which supplies a plurality of active termination control signals to said memory circuits according to an operational mode of said memory circuits;

wherein each of the plurality of memory circuits includes a termination resistor and a control circuit, and wherein said control circuit receives the active termination control signal supplied to the memory circuit thereof, and selectively

switches on and off the termination resistor in response to the active termination control signal;

wherein said control circuit includes a synchronous input buffer and an asynchronous input buffer which each receive the active termination control signal, and a switching circuit which selects one of an output of said synchronous input buffer or an output of said asynchronous input buffer according to an operational mode of the memory circuit containing said buffer circuit, and wherein an output of said switching circuit controls an on and off state of said termination resistor.

12. The memory system of claim 11, wherein the switching circuit selects the output of the synchronous input buffer when the memory circuit is in an active operational mode, and selects the output of the asynchronous input buffer when the memory circuit is in a standby or power-down operational mode.

13. The memory system of claim 11, further comprising a plurality of memory modules each having at least one of the plurality of memory circuits

mounted thereto, wherein the plurality of active termination control signals are supplied to the memory circuits of the plurality of memory modules, respectively, such that the memory circuits of each memory module receive a same one of the plurality of active termination control signals.

14. The memory system of claim 12, further comprising a plurality of memory modules each having at least one of the plurality of memory circuits mounted thereto, wherein the plurality of active termination control signals are individually supplied to the memory circuits of the plurality of memory modules, respectively, such that the memory circuits of each memory module receive a different one of the plurality of active termination control signals.

15. The memory system of claim 12, wherein the plurality of memory circuits are DRAM circuits mounted in dual in-line memory modules.

16. The memory system of claim 11, wherein the plurality of active

termination control signals are individually supplied to the memory circuits of each side of a plurality of dual in-line memory modules, respectively, such that each side of the dual in-line memory modules receive a different one of the plurality of active termination control signals.

17. A memory system comprising:

a bus line;

a plurality of memory modules coupled to said bus line, wherein each of the memory modules has at least two sides, and wherein a plurality of memory circuits are mounted on each side of the memory modules; and

a chip set, coupled to said bus line, which supplies a plurality of active termination control signals to said memory module;

wherein an operational mode of the plurality of memory circuits mounted on each side of the memory modules are controlled individually;

wherein the plurality of active termination control signals are supplied to the memory circuits of the plurality of memory modules, respectively, such that the

memory circuits of each side of the memory modules receive a same one of the plurality of active termination control signals;

wherein each of the plurality of memory circuits includes a termination resistor, a control circuit, and a mode register which stores data indicative of an operational mode of the memory modules;

wherein said control circuit includes a synchronous input buffer and an asynchronous input buffer which each receive the active termination control signal, and a switching circuit which selects one of an output of said synchronous input buffer or an output of said asynchronous input buffer according to the date of the mode register, and wherein an output of said switching circuit controls an on/off state of said termination resistor.

18. The memory system of claim 17, wherein said switching circuit selects the output of said synchronous input buffer when the plurality of memory circuits mounted on at least one side of a corresponding memory module are in an active operational mode, and selects the output of said asynchronous input buffer when

the plurality of memory circuits mounted on both sides of the corresponding memory module are in a standby or power-down operational mode.

19. A method for controlling an operation of a memory circuit:

applying an input signal to a synchronous input buffer and to an asynchronous input buffer of the memory circuit; and

selectively outputting an output of the synchronous input buffer or an output of the asynchronous input buffer according to an operational mode of the memory circuit.

20. The method of claim 19, further comprising enabling and disabling a termination resistance of the memory circuit according to the selected output of the synchronous input buffer or the asynchronous input buffer.

21. The circuit of claim 20, further comprising receiving an operational mode signal which is supplied externally of the memory circuit, wherein a value of

the operational mode signal controls the selective outputting of the output of the synchronous input buffer or the output of the asynchronous input buffer.

22. The circuit of claim 20, further comprising receiving a value stored in a mode register of the memory circuit, wherein the value of the mode register controls the selective outputting of the output of the synchronous input buffer or the output of the asynchronous input buffer..

23. A method of controlling an on/off state of a termination resistor of a memory circuit, said method comprising:

supplying an active termination control signal to both a synchronous input buffer and an asynchronous input buffer of the memory circuit;

selecting an output of the synchronous input buffer when the memory circuit is in an active operational mode, and selecting an output of the asynchronous input buffer when the memory circuit is in a standby or power-down operational mode; and

setting an on/off state of the termination resistor according to the selected one of the output of the synchronous input buffer or the output of the asynchronous input buffer.

24. A method of controlling a plurality of termination resistors of a respective plurality of memory circuits in a memory system, the memory system having a plurality of memory modules connected to a data bus, each of the memory modules for mounting at least one of the plurality of memory circuits thereto, said method comprising:

supplying an active termination control signal to both a synchronous input buffer and an asynchronous input buffer of each of the memory circuits of each of the memory modules;

selecting, in each memory circuit, an output of the synchronous input buffer when the memory circuit is in an active operational mode, and selecting an output of the asynchronous input buffer when the memory circuit is in a standby or power-down operational mode; and

setting, in each memory circuit, an on/off state of the termination resistor according to the selected one of the output of the synchronous input buffer or the output of the asynchronous input buffer.

25. A method of controlling a plurality of termination resistors of a respective plurality of memory circuits in a memory system, the memory system having at least a first memory module and a second memory module connected to a data bus, each of the memory modules for mounting at least one of the plurality of memory circuits thereto, said method comprising:

transmitting, in response to a read/write instruction of the first memory module, an active termination control signal to the memory circuits of each of the second memory module;

supplying the active termination control signal to both a synchronous input buffer and an asynchronous input buffer of each of the memory circuits of the second memory module;

selecting, in each of the memory circuits of the second memory module, an

output of the synchronous input buffer when the second memory module is in an active operational mode, and selecting an output of the asynchronous input buffer when the second memory module is in a standby or power-down operational mode; and

setting, in each memory circuit of the second memory module, an on/off state of the termination resistor according to the selected one of the output of the synchronous input buffer or the output of the asynchronous input buffer.